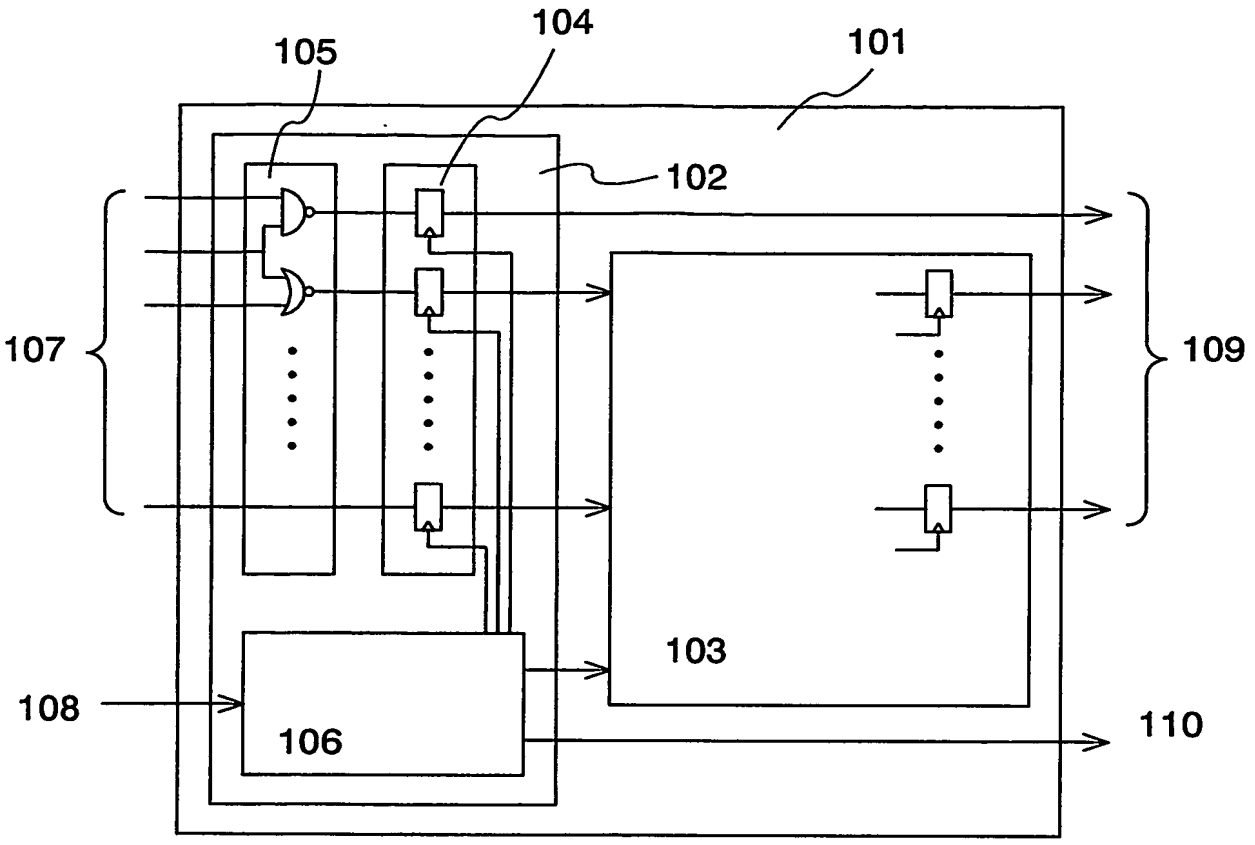
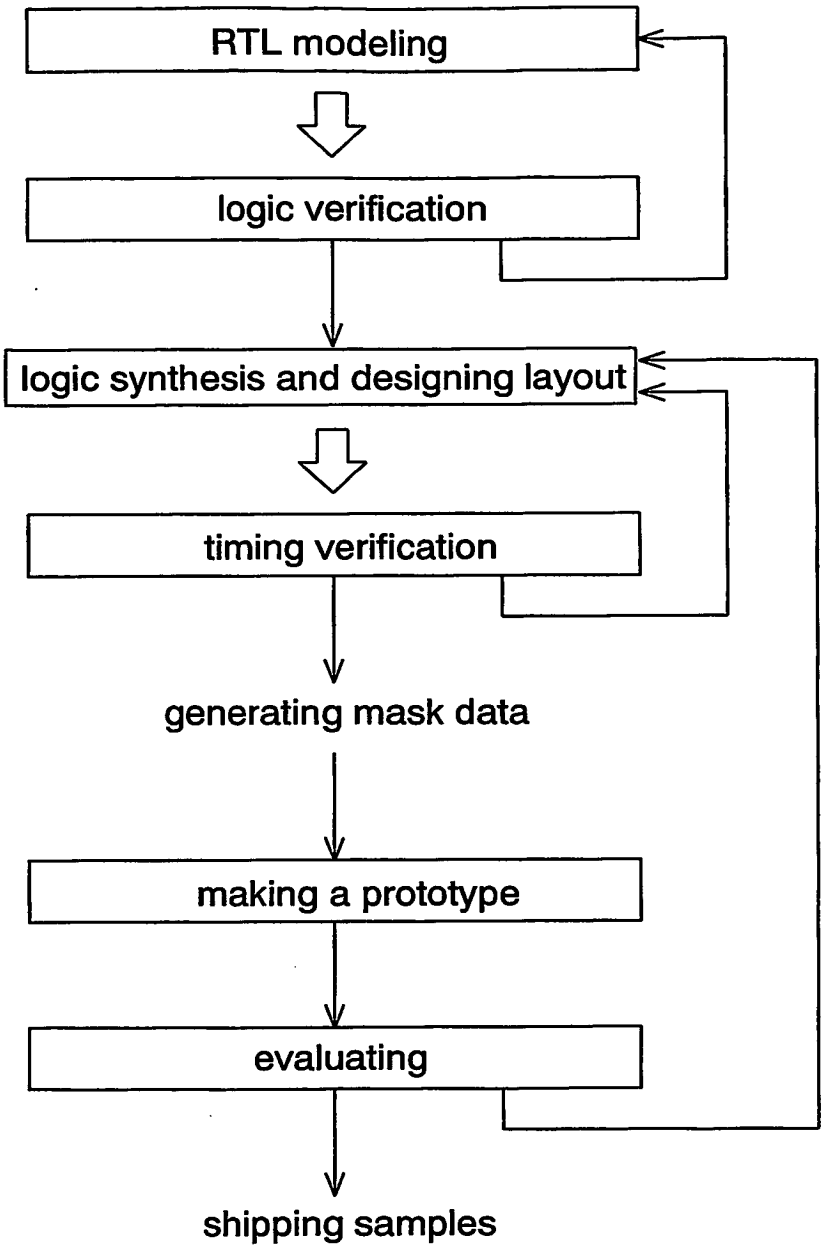


FIG. 1



PRIOR ART

FIG. 2

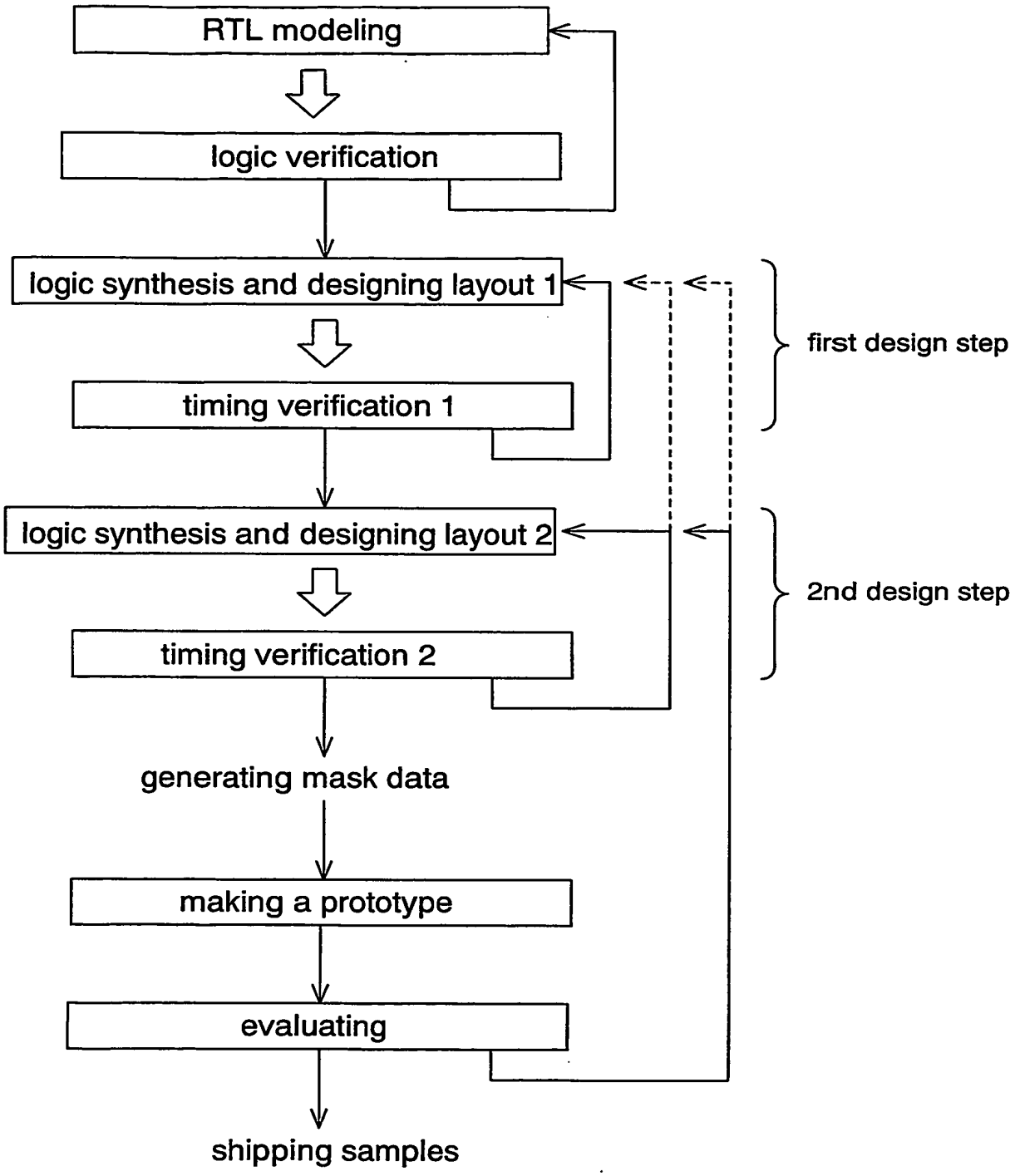

RTL modeling
logic verification
logic synthesis and designing layout 1
timing verification 1
logic synthesis and designing layout 2
timing verification 2
generating mask data
making a prototype
evaluating
shipping samples
first design step
2nd design step

FIG. 3

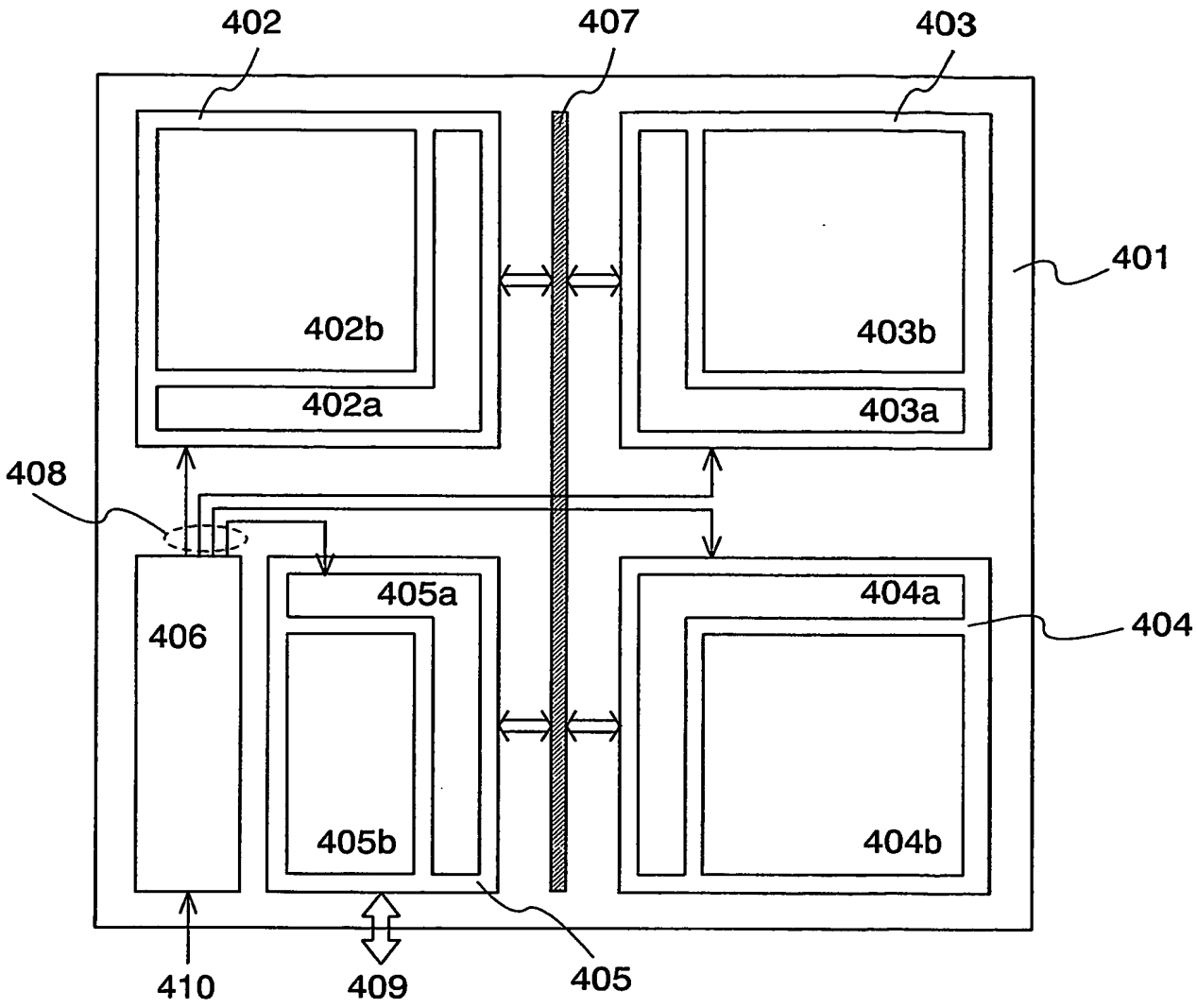

402
407
403
401
402b
403b
402a
403a
408
405a
404a
406
404
405b
404b
410
409
405

FIG. 4

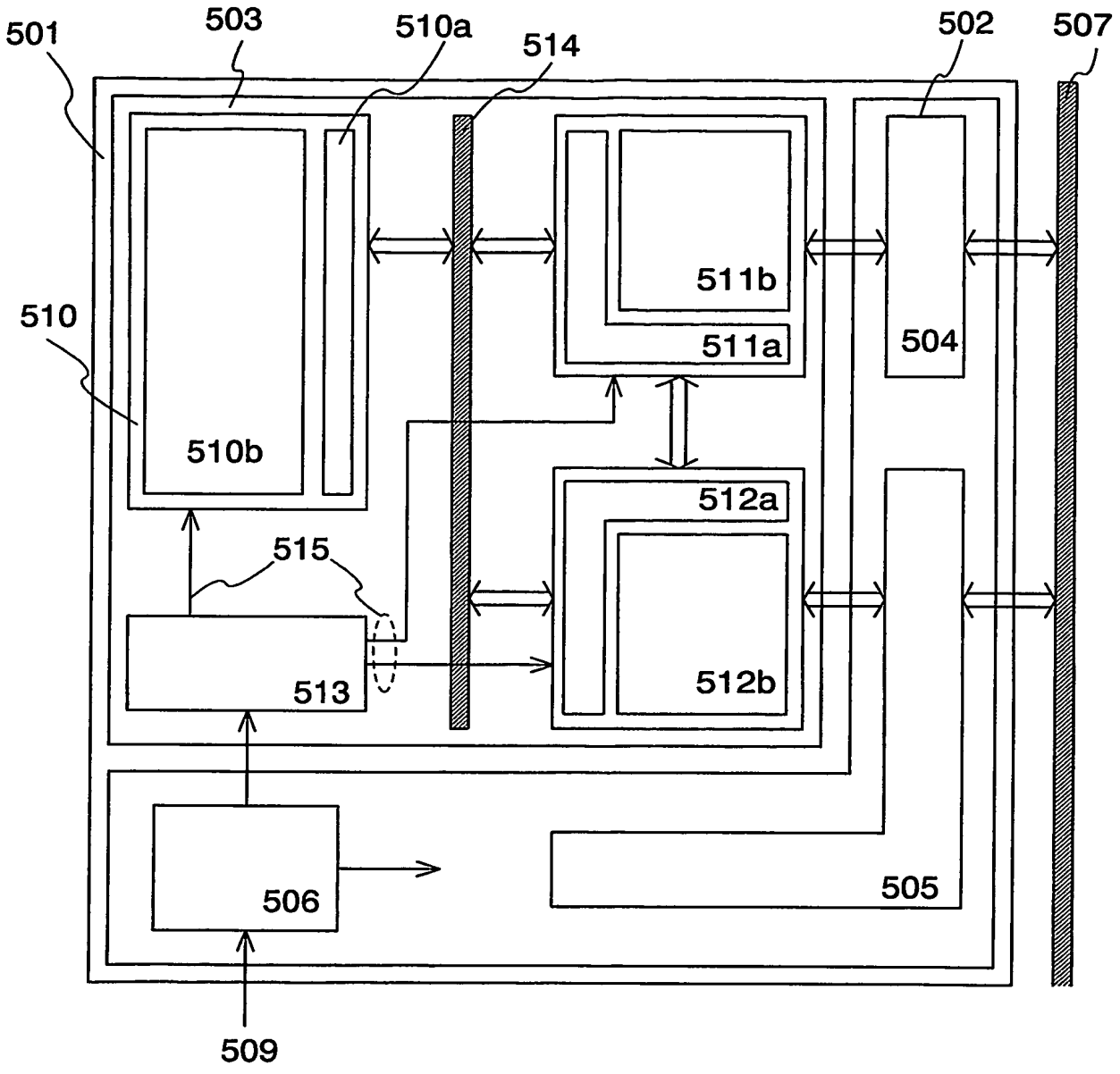

501
503
510a
514
502
507
510
511b
511a
504
510b
512a
515
513
512b
506
505
509

FIG. 5

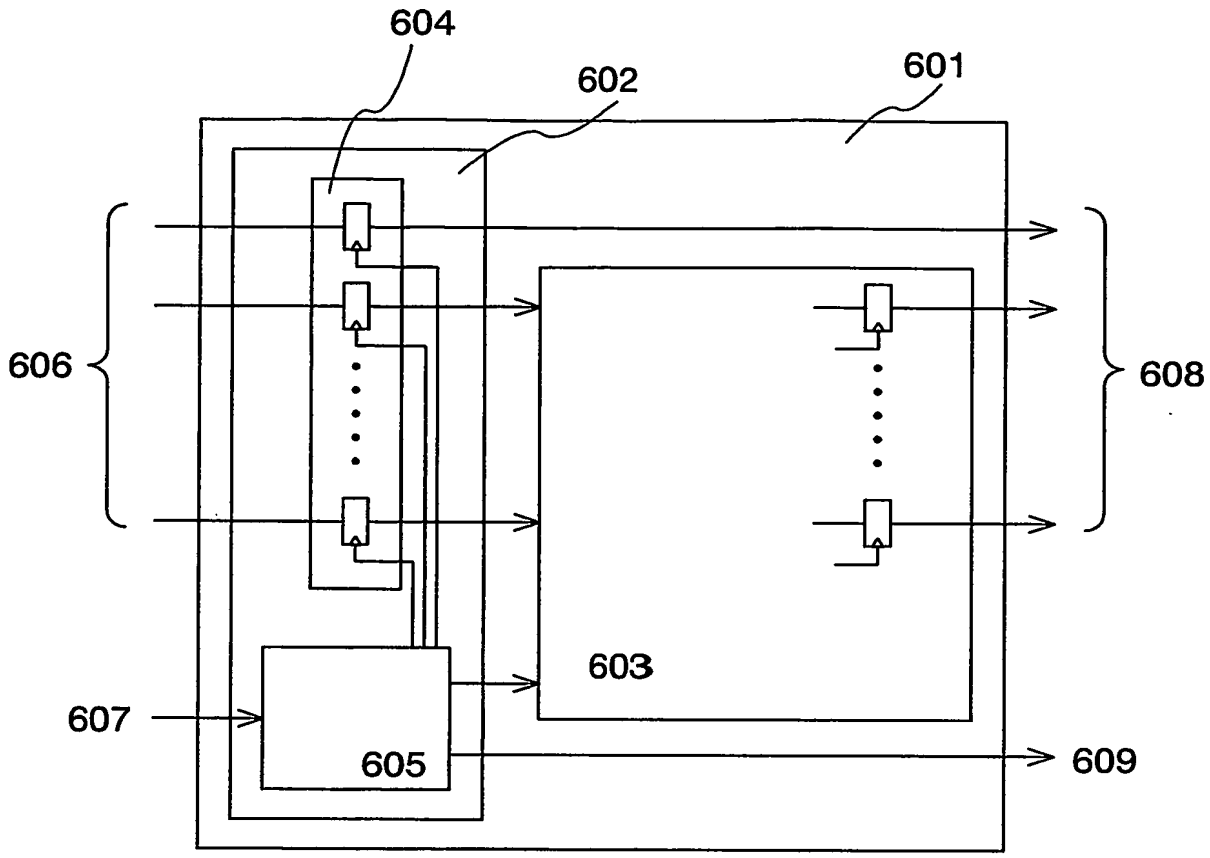


FIG. 6

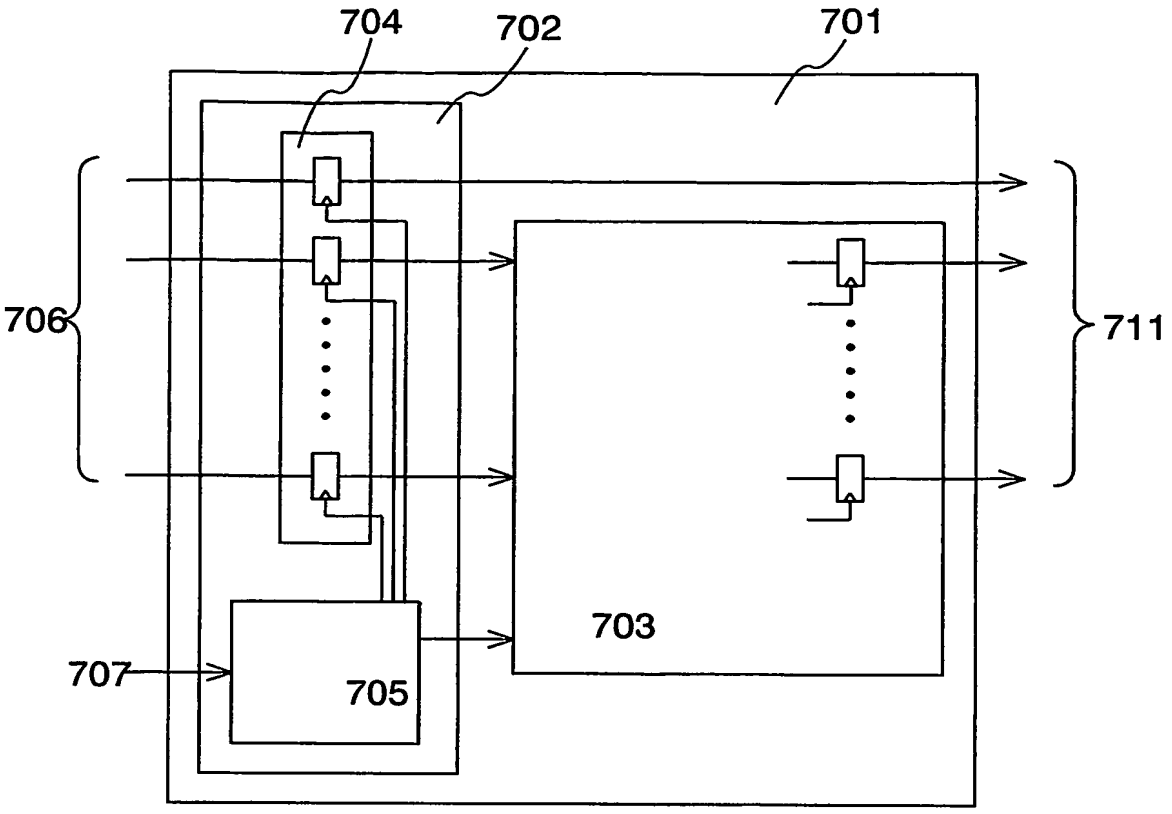


FIG. 7A

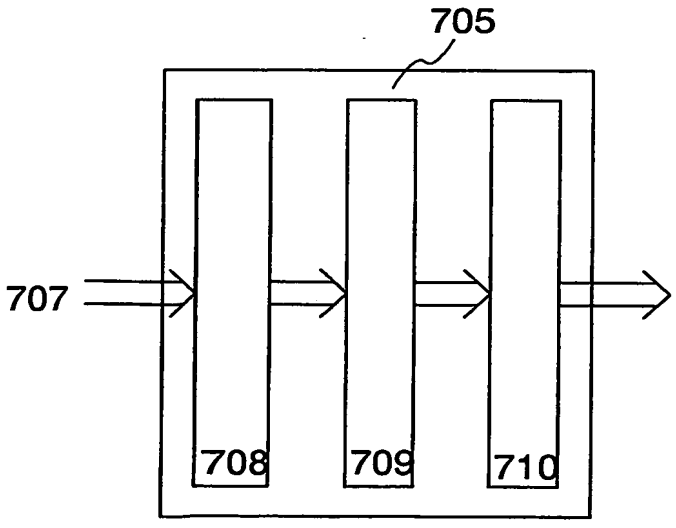


FIG. 7B

EXPLANATION OF REFERENCES

101: logic block 102: first logic circuit 103: second logic circuit 104: first group of registers 105: logic circuit 106: control circuit 107: input data 108: input control signal 109: output data 110: output control signal 401: semiconductor integrated circuit 402: logic block 402a: first logic circuit 402b: second logic circuit 403: logic block 403a: first logic circuit 403b: second logic circuit 404: logic block 404a: first logic circuit 404b: second logic circuit 405: logic block 405a: first logic circuit 405b: second logic circuit 406: control signal generating circuit 407: data lines 408: control lines 501: logic block 502: first logic circuit 503: second logic circuit 504: first group of registers 505: first group of registers 506: control circuit 507: data lines 509: control lines 510: logic sub-block 511a: third logic circuit 511b: fourth logic circuit 512a: third logic circuit 512b: fourth logic circuit 513: control circuit 514: data lines 515: control lines 601: logic block 602: first logic circuit 603: second logic circuit 604: first group of resistors 605: control circuit 606: input data 607: input control signal 608: output data 609: output control signal 701: logic block 702: first logic circuit 703: second logic circuit 704: first group of registers 705: control circuit 706: input data 707: input control signal 708: output data 709: control signal generating circuit 710: timing adjustment circuit